Chrontel

CH7035B DVI Transmitter

FEATURES

- DVI encoder support up to 1080p
- SPDIF audio interface supports either 16-bit or 20bit stereo data for up to 192kHz/2ch
- Support 2 channel I2S digital audio input for up to 24-bit data stream (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHzand 192kHz)
- DDC master for reading EDID
- Hot plug detection for DVI
- On-chip frame buffer supports frame rate conversion provides the graphic controller the flexibility of video timing output
- Advanced scaling engine to upsize/downsize input resolution for DVI display up to 1080p
- Supports 8/12/16/18/24-bit parallel interface input for either RGB format (RGB-565, RGB-666 or RGB-888 and etc.) or YCrCb format (ITU-R 656 or ITU-R 601). 80/86 MPU interface and DE only mode are also supported.
- Wide range of input resolutions support for up to 1366x768 (i.e. 640x480, 720x480, 720x576, 800x600, 1024x600, 1024x768, 1280x800, and etc.)
- Image display rotation support at 90/180/270 degree or flipped in horizontal/vertical position
- Pixel clock input frequency support for up to 165 MHz
- IO Supply Voltages from 1.2V to 3.3V and SPC/SPD Supply Voltages from 1.8V to 3.3V.
- Programmable power management
- Device fully programmable through serial port or can automatically load firmware from Chrontel Boot ROM (CH9904)
- Offered in a 88-pin QFN package

APPLICATION

- Mobile Phones / Tablet Devices
- Smartbooks / Ultrabooks
- Digital Cameras
- DVD Players or Recorders
- Portable Media Players

GENERAL DESCRIPTION

The Chrontel CH7035B is specifically designed for consumer electronics device and PC markets which multiple high definition content display formats are required. With its advanced video encoder, flexible scaling engine and easy-to-configure audio interface, the CH7035B satisfies manufactures' products display requirements and reduce their costs of development and time-to-market.

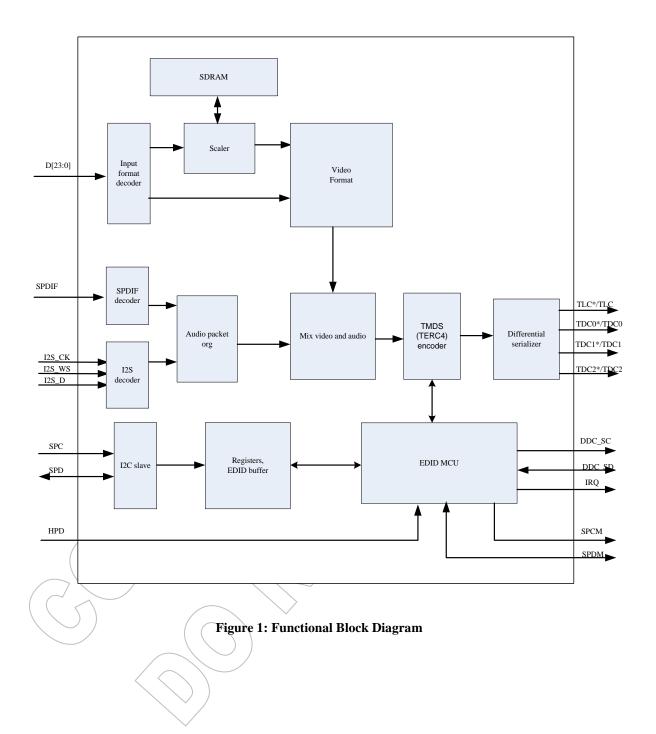
The CH7035B's 24-bit parallel bus accepts a wide range of input data formats from the graphic controller. The built-in video port supports 8/12/16/18/24-bit data interface as well as 80/86 MPU interface. The video format conversion module is capable of translating digital RGB-565, RGB-666, RGB-888 or YCrCb (ITU-R 656, ITU-R 601) signal to the DVI signal, combining with the audio stream. The device's video capture block supports input display resolution for up to 1366x768 which can be either interlaced or non-interlaced timing.

The CH7035B has incorporated a high speed SDRAM to help manufactures design their product to achieve simultaneous LCD and DVI display. A sophisticated frame rate conversion technology in the device's scaler retrieves LCD data from the SDRAM frame buffer, and increases the native display resolution up to 1080p DVI display. Furthermore, the CH7035B provides additional image manipulation features including image rotation, which can be implemented through programming internal registers.

The device supports both SPDIF and 2-channel I S digital audio input. Its high fidelity audio decoder engine has the capability of sampling audio frequency for up to 192k/2ch. The SPIDF supports PCM encoded data and compressed audio including Dolby Digital and DTS.

The CH7035B has an image enhancement function that can fine tune brightness, contrast, hue and saturation down to the pixel-level.

When the HPD signal is asserted, the CH7035B will automatically generate an interrupt to the processor. A build-in DDC port can read the EDID data from DVI monitor through programming. registers by the processor.



1.0 PIN-OUT

1.1 Package Diagram

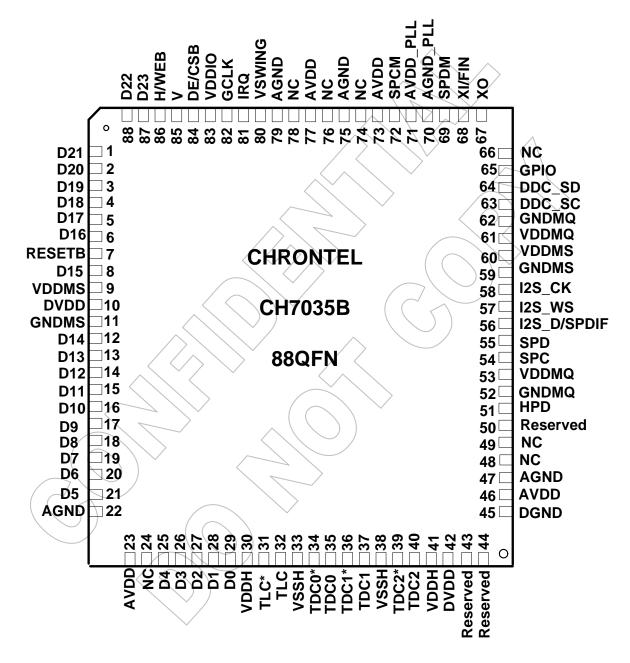


Figure 2: 88 pin QFN Package (Top View)

1.2 Pin Description

Table 1: Pin Name Descriptions (QFN88 Package)

| Pin # | Туре | Symbol | Description | | | |
|--------|----------|--|---|--|--|--|
| 1~6,8, | In | D[23:0] | Data Input | | | |
| 12~21, | | | These pins accept 24 data input lines from a digital video port of a | | | |
| 25~29, | | | graphics controller. The swing is defined by VDDIO. | | | |
| 87~88, | | | All the unused Data input pins should be pulled low with $10K\Omega$ | | | |
| 07 00, | | | resistors or shorted to Ground directly. | | | |
| 7 | In | RESETB | Reset Input | | | |
| | | | When this pin is low, the device is held in the power-on reset | | | |
| | | | condition. When this pin is high, reset is controlled through the serial | | | |
| | | | port. | | | |
| 31,32 | Out | TLC*,TLC | DVI Clock Outputs | | | |
| 01,02 | out | 120 ,120 | These pins provide the differential clock output for the DVI. | | | |
| 34,35 | Out | TDC0*,TDC0 | DVI Data Channel 0 Outputs | | | |
| 51,55 | Out | 1000,1000 | These pins provide the DVI differential outputs for data channel 0 | | | |
| 36,37 | Out | TDC1*,TDC1 | DVI Data Channel 1 Outputs | | | |
| 50,57 | Out | | These pins provide the DVI differential outputs for data channel 1 | | | |
| 39,40 | Out | TDC2*,TDC2 | DVI Data Channel 2 Outputs | | | |
| 39,40 | Out | IDC2 ⁺ ,IDC2 | These pins provide the DVI differential outputs for data channel 2 | | | |
| 40 | NT/A | D 1 | | | | |
| 43 | N/A | Reserved | Reserved | | | |
| | N. 7 / 4 | | This pin should connect to DVDD directly | | | |
| 44 | N/A | Reserved | Reserved | | | |
| | | | This pin should connect to DGND directly | | | |
| 50 | N/A | Reserved | Reserved | | | |
| | | | This pin should be left open or pulled low with a 10 K Ω resistor in the | | | |
| | | $\langle \langle \cdot \rangle \rangle \vee$ | application. | | | |
| 51 | In 🧹 | HPD | Hot Plug Detect | | | |
| | | $\langle / \rangle \rangle$ | This input pin determines whether the DVI output driver is connected | | | |
| | | \rightarrow \checkmark | to a DVI monitor. This pin should be pull low with 47 K Ω Resistor. | | | |
| 54 | In | SPC | Serial Port Clock Input | | | |
| | | $\langle \rangle$ | This pin functions as the clock pin of the serial port. External pull-up | | | |
| (| ()) | \sim | $6.8 \text{ K}\Omega$ resister is required. | | | |
| 55 | In/out | SPD | Serial Port Data Input / Output | | | |
| | | | This pin functions as the bi-directional data pin of the serial port. | | | |
| | | | External pull-up 6.8 K Ω resister is required. | | | |
| 56 | In | I2S_D/SPDIF | I2S Data input or SPDIF Audio Signal Input | | | |
| 50 | / | | In default, this pin is configured to SPDIF audio signal input. The | | | |
| | | $\square \square \square \square$ | signal level is 0-2.5V. | | | |
| | | | I2S audio input can be configured through programming CH7035B | | | |
| | - | $\langle \langle \rangle \rangle$ | registers. | | | |
| 57 | In | I2S_WS | I2S Channel Select Signal | | | |
| 58 | In | I2S_CK | I2S Clock Signal | | | |
| | | | | | | |
| 63 | Out | DDC_SC | Routed Serial Port Clock Output to DDC | | | |
| | | | This pin functions as the clock bus of the serial port to DDC receiver. | | | |
| | | | This pin will require a pull-up 1.8 K Ω resistor to the desired voltage | | | |
| | | | level. A pull-low resistor 10 K Ω to ground if unused. | | | |
| 64 | In/out | DDC_SD | Routed Serial Port Data to DDC | | | |
| | | | This pin functions as the bi-directional data pin of the serial port to | | | |
| | | | DDC receiver. This pin will require a pull-up 1.8 K Ω resistor to the | | | |
| | | | desired voltage level. A pull-low resistor 10 K Ω to ground if unused | | | |
| 65 | In/out | GPIO | General Purpose Input Output | | | |
| 67 | Out | XO | Crystal Output | | | |
| ~ ' | 0 | | A parallel resonance crystal should be attached between this pin and | | | |
| | 1 | l | 1.1. paratier resonance erjour should be attached between this pill and | | | |

| Matrix Average and the second s | Pin # | Туре | Symbol | Description | | | |
|--|-------------|-------------------|----------------------------|---|--|--|--|
| 68 In XL/FIN Crystal Juput / External Reference Input A parallel resonance crystal should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XL/FIN input. 69 In/Out SPDM Routed Serial Port Data to CH9904 BOOT ROM This pin functions as the bi-directional data pin of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KO resistor to the desired voltage level. A pull-low resistor 10K to ground if mused. 72 Out SPCM Routed Serial Port Clock Output to CH9904 BOOT ROM This pin functions as the clock bas of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KO resistor to the desired voltage level. A pull-low resistor 10 KO to ground if mused. 80 In VSWING VSWING 81 Out IRQ Programmed Interrupt output. 82 In GCLK External Clock lignuts The input is the clock signal input to the device for use with the H. V, DE and D[2:30] data. 84 In DE/CSB Data Input Indicator When the pin is high, the input data is active. When the pin is high, the input data is active. When the pin is high, the input data is active. When the pin is high, the input data is active. When the SVO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 VDDIO. 85 In/out HWEB Horizontal Sync Input / Output When the SVO control bit is low, the input a vertical sync pulse. The output is driven fro | | | | | | | |
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| 80 In Out SPDM Routed Scrill Port Data to CH9904 BOOT ROM 72 Out SPCM Routed Scrill Port Data to CH9904 BOOT ROM 72 Out SPCM Routed Scrill Port Clock Output to CH9904 BOOT ROM 72 Out SPCM Routed Scrill Port Clock Output to CH9904 BOOT ROM 71 Out SPCM Routed Scrill Port Clock Output to CH9904 BOOT ROM 70 Out SPCM Routed Scrill Port Clock Output to CH9904 BOOT ROM 71 Dut SPCM Routed Scrill Port Clock Output to CH9904 BOOT ROM 70 Out SPCM Routed Scrill Port Clock Output to CH9904 BOOT ROM 70 Out SPCM Routed Scrill Port Clock Output to CH9904 BOOT ROM 70 This pin sets the swing level of the DVI outputs. A 1.2 KW (U. %) resistor should be connected between this pin and AGND using short and wide traces. 81 Out IRQ Programmed Interrupt output. 82 In GCLK External Clock Inputs 84 In DE/CSB Data Input Indicator 9 Data Input Indicator When the pin is high, the input data is blanking. 11 is also a CSB signal input of MPU interface The | 68 | In | XI/FIN | | | | |
| def In Yout SPDM Routed Serial Port Data to CH9904 BOOT ROM This pin functions as the bi-directional data pin of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10K to ground if mused. 72 Out SPCM Routed Serial Port Clock Output to CH9904 BOOT ROM This pin functions as the clock bus of the serial port to CH9904 BOOT ROM. This pin functions as the clock bus of the serial port to CH9904 BOOT ROM. This pin functions as the clock bus of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused. 80 In VSWING VSWING 81 Out IRQ Programmed Interrupt output. 82 In GCLK External Clock Inputs The input is the clock signal input on the device for use with the H, V, DE and D[23:0] data. 84 In DE/CSB Data Input Indicator When the pin is high, the input data is active. When the pin is high, the input data is balaking. It is also a CSB signal input of MPU interface The amplitude will be VV VDDIO. 85 In/out V Vertical Sync Input/Votput When the SYO control bit is how, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of MPU interface. | | | | | | | |
| 69 In'Out SPDM Routed Serial Port Data to CH9904 BOOT ROM This pin functions as the bi-directional data pin of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10K to ground if unused. 72 Out SPCM Routed Serial Port Clock Output to CH9904 BOOT ROM This pin functions as the block bus of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused. 80 In VSWING This pin sets the swing level of the DVI outputs. A 1.2 KW (1.%) resistor-should be connected between this pin and AGND using short and wide traces. 81 Out IRQ Programmed Interrupt output. 82 In GCLK External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data. Data Input Indicator 84 In DE/CSB Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. It is also aCSB signal input of MPU interface The amplitude will be 0V to VDDIO. 85 In/out V Vertical Sync Input/Output 86 In/out V Vertical Sync Input / Output 86 In/out H/WEB Horizontal Sync Input / Output 86 In/out | | | | | | | |
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| CH9904 BOOT ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10K to ground if unuscd. 72 Out SPCM Routed Serial Port Clock Output to CH9904 BOOT ROM This pin functions as the lock bus of the serial port to CH9904 BOOT ROM. This pin mull require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused. 80 In VSWING VSWING 81 Out IRQ Programmed Interrupt output. 82 In GCLK External Clock Input 84 In DECSB Data Input Indicator When the pin is high, the input data is balaking. When the pin is high, the input data is balaking. When the pin is high, the input data is balaking. When the SYO control bit is low, this pin accepts a vertical sync input for use with the iNY oction bit is low, this pin accepts a vertical sync input for use with the SYO control bit is low, this pin accepts a vertical sync input for use with the iNY oction bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 10 vDDIO. When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is low, the over will output a vertical sync pulse. The output is driven from the VDDIO supply. It is also the WED synchy (J.3V) 86 In/out H/WEB Horizo | 69 | In/Out | SPDM | | | | |
| it to desired voltage level. A pull-low resistor 10K to ground if unused. 72 Out SPCM Routed Serial Port Clock Output to CH9904 BOOT ROM This pin functions as the clock bus of the serial port to CH9904 BOOT ROM This pin will require a pull-up of 8 KΩ resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused. 80 In VSWING VSWING 81 Out IRQ Programmed Interrupt output. 82 In GCLK External Clock Inputs 84 In DECSB Data Input Indicator When the pin is high, the input data is active. When the pin is high, the input data is blanking. 85 Infout V Vertical Sync Input/Output 86 Infout V Vertical Sync Input/Output 87 Infout V Vertical Sync Input/Output 88 Infout V Vertical Sync Input/Output When the SV control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be to VDDIO. 86 Infout When the SV control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be to VDDIO. 86 < | | | | | | | |
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| BitThis pin functions as the clock bus of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused.80InVSWINGVSWING This pin sets the swing level of the DVI outputs. A 1.2 KW (1%) resistor-should be connected between this pin and AGND using short and wide traces.81OutIRQProgrammed Interrupt output.82InGCLKExternal Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D12:301 data.84InDE/CSBData Input Indicator When the pin is high, the input data is blanking. It is also a CSB signal input of MPU interface The amplitude will be 0V to VDDIO.85In/outVVertical Sync Inpit/Output When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply. When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input of MPU interface. The anglitude will be 0V to DDIO.86In/outH/WEBHorizontal Sync Inpit/Output When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of MPU interface.24, 48, 49, R6N/ANCNot Connect These pins should be left open.78OwerVDDMSSDRAM Ground10,42PowerVDDDDigital Forund23, 46, 73, PowerAGNDAnalog Ground <t< td=""><td>72</td><td>Out</td><td>SPCM</td><td></td></t<> | 72 | Out | SPCM | | | | |
| ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused.80InVSWINGVSWING81OutIRQProgrammed Interrupt output.82InGCLKExternal Clock isgnal input to the device for use with the H, V, DE and D[23:0] data.84InDE/CSBData Input Indicator When the pin is high, the input data is active. When the pin is high, the input data is active. When the pin is high, the input data is active. When the pin is high, the input data is active. When the pin is high, the input data is active. When the pin is high, the input data is active. When the pin is high, the input data is active. When the pin is high, the input data is active. When the pin is high, the device and unput of DUDIO.85In/outVVertical Sync Input/Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input is the input ata. The amplitude will be 0 to VDDIO. When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is low, this pin accepts a horizontal sync pulse. The output is driven | | | | | | | |
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| 81 Out IRQ Programmed Interrupt output. 82 In GCLK External Clock Inputs 84 In DE/CSB Data Input Indicator 84 In DE/CSB Data Input Indicator 85 Infout V When the pin is high, the input data is active. 85 In/out V Vertical Sync Input/Output 86 In/out V Vertical Sync Input/Output 86 In/out H/WEB Horizontal Sync Input/Output When the SYO control bit is bigh, the device will output a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. 86 In/out H/WEB Horizontal Sync Input/Output When the SYO control bit is high, the device will output a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. 86 In/out H/WEB Horizontal Sync Input / Output When the SYO control bit is high, the device will output a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. 86 In/out H/WEB Horizontal Sync Input / Output When the SYO control bit is high, the device will output a horizontal sync uput so the will be otor VDDIO. When the SYO control bit is hig | 80 | In | VSWING | VSWING | | | |
| AGND using short and wide traces.81OutIRQProgrammed Interrupt output.82InGCLKExternal Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.84InDE/CSBData Input Indicator When the pin is high, the input data is active. When the pin is high, the input data is blanking. It is also a CSB signal input of MPU interface The amplitude will be 0V to VDDIO.85In/outVVertical Sync Input/Output When the sync control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO.86In/outH/WEBHorizontal Sync Input/Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is low, this pin accepts a horizontal sync input for use with the SYO control bit is low the will be 0 to VDDIO. When the SYO control bit is low, this pin accepts a horizontal sync input for use with the signal of MPU interface.24, 48, 49, 66, 74, 76, 78N/ANCNot Connect These pins should be left open. 789,60PowerVDDMSSDRAM Ground10,42PowerDGNDDigital Ground23, 46, 73, 79PowerAGNDAnalog Ground24, 47, 75, 79PowerAGNDAnalog Ground </td <td></td> <td></td> <td></td> <td>This pin sets the swing level of the DVI outputs. A 1.2 KW</td> | | | | This pin sets the swing level of the DVI outputs. A 1.2 KW | | | |
| 81 Out IRQ Programmed Interrupt output. 82 In GCLK External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data. 84 In DE/CSB Data Input Indicator When the pin is high, the input data is blanking. It is also a CSB signal input of MPU interface The amplitude will be 0V to VDDIO. 85 In/out V Vertical Sync Input/Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the imput data. The amplitude will be 0 to VDDIO. 86 In/out H/WEB Horizontal Sync Input/Output When the SYO control bit is low, this pin accepts a horizontal sync pulse. The output is driven from the VDDIO supply. 86 In/out H/WEB Horizontal Sync Input/Output When the SYO control bit is low, this pin accepts a horizontal sync pulse. The output is driven from the VDDIO supply. 86 In/out H/WEB Not Connect These pins should be left open. 78 9,60 Power VDDMS SDRAM Power Supply (3.3V) 59,11 Power DGND Digital Ground 10,42 Power DGND Digital Ground 23, 46, 73, Power AGND Analog Ground 24, 47, 75, Power AGND Analog Ground | | | | (1 %) resistor should be connected between this pin and | | | |
| 82 In GCLK External Clock Inputs 84 In DE/CSB Data Input Indicator When the pin is high, the input data is active. When the pin is high, the input data is blanking. It is also a CSB signal input of MPU interface 85 In/out V Vertical Sync Input/Output 86 In/out V Vertical Sync Input/Output 86 In/out H/WEB Horizontal Sync Input / Output 86 In/out H/WEB Horizontal Sync Input / Output 87 N/A NC Nen the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. 86 In/out H/WEB Horizontal Sync Input / Output When the SYO control bit is high, the device will output a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. 86 In/out H/WEB Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. 87 In/out H/WEB Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. | | | 4 | AGND using short and wide traces. | | | |
| 84InDE/CSBData Input Is the clock signal input to the device for use with the H, V, DE and D[23:0] data.84InDE/CSBData Input Indicator When the pin is high, the input data is active. When the pin is high, the input data is blanking. It is also a CSB signal input of MPU interface The amplitude will be 0V to VDDIO.85In/outVVertical Sync Input/Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO.86In/outH/WEBHorizontal Sync Input / Output When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.86In/outH/WEBHorizontal Sync Input / Output When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply.86In/outH/WEBHorizontal Sync Input / Output When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of MPU interface.24, 48, 49, 0,60PowerVDDMSSDRAM Power Supply (3.3V)59,11PowerGNDMSSDRAM Ground10,42PowerDGNDDigital Power Supply (1.8V)45PowerDGNDDigital Ground23, 46, 73, PowerAGNDAnalog Ground7724, 47, 75, PowerAGNDAnalog Ground | 81 | Out | IRQ | Programmed Interrupt output. | | | |
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| 84 In DE/CSB Data Input Indicator 84 In DE/CSB Data Input Indicator When the pin is low, the input data is active. When the pin is low, the input data is blanking. It is also a CSB signal input of MPU interface The amplitude will be 0V to VDDIO. 85 In/out V Vertical Sync Input/Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply. 86 In/out H/WEB Horizontal Sync Input / Output When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. 86 In/out H/WEB Horizontal Sync Input / Output When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of MPU interface. 24, 48, 49, 66, 74, 76, 78 N/A NC Not Connect These pins should be left open. 78 9.60 Power VDDMS SDRAM Ground 10.42 Power DVDD Digital Ground 10.42 Power DGND Digital Ground 23, 46, 73, 79 Power AGND Analog Ground | | | $ \land \land \land$ | | | | |
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| It is also a CSB signal input of MPU interface The amplitude will be 0V to VDDIO.85In/outV85In/outV86In/outH/WEB86In/outH/WEB86In/outH/WEB86In/outH/WEB86In/outH/WEB86N/AN/C86N/AN/C87N/A88N/A89N/A89,60Power9,60Power9,60Power9,60Power9,11Power10,42Power23, 46, 73, PowerDGND23, 46, 73, PowerAGND22, 47, 75, PowerAGND24, 47, 75, PowerAGND24, 47, 75, PowerAGND25, 47, 75, PowerAGND24, 47, 75, PowerAGND25, 47, 75, PowerAGND26, 47, 75, PowerAGND27, 47, 75, PowerAGND28, 47, 75, PowerAGND29, 50Power29, 50Power24, 47, 75, PowerAGND25, 47, 75, PowerAGND26, 47, 75, PowerAGND27, 47, 75, PowerAGND28, 47, 75, PowerAGND29, 50Power29, 50Power20, 47, 75, PowerAGND21, 47, 75, PowerAGND22, 47, 75, PowerAGND45Power45Power46Power47Power <td></td> <td></td> <td>$\langle \rangle \rangle$</td> <td></td> | | | $ \langle \rangle \rangle$ | | | | |
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| 86In/outH/WEBHorizontal Sync Input / Output When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.86In/outH/WEBHorizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of MPU interface.24, 48, 49, 66, 74, 76, 78N/ANCNot Connect These pins should be left open.9,60PowerVDDMSSDRAM Power Supply (3.3V)59,11PowerGNDMSSDRAM Ground10,42PowerDVDDDigital Power Supply (1.8V)45PowerDGNDDigital Ground23, 46, 73, 79PowerAGNDAnalog Ground22, 47, 75, 79PowerAGNDAnalog Ground | | \frown | | When the SYO control bit is low, this pin accepts a vertical sync input | | | |
| 86In/outH/WEBHorizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of MPU interface.24, 48, 49, 66, 74, 76, 78N/ANCNot Connect These pins should be left open.9,60PowerVDDMSSDRAM Power Supply (3.3V)59,11PowerGNDMSSDRAM Ground10,42PowerDVDDDigital Power Supply (1.8V)45PowerDGNDDigital Ground23, 46, 73, 79PowerARIDAnalog Ground22, 47, 75, 79PowerAGNDAnalog Ground | (| \frown | \searrow | | | | |
| 86In/outH/WEBHorizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of MPU interface.24, 48, 49, 66, 74, 76, 78N/A NCNCNot Connect These pins should be left open.9,60PowerVDDMSSDRAM Power Supply (3.3V)59,11PowerGNDMSSDRAM Ground10,42PowerDVDDDigital Power Supply (1.8V)45PowerDGNDDigital Ground23, 46, 73, 77PowerANDDAnalog Power Supply (3.3V)22, 47, 75, 79PowerAGNDAnalog Ground | | $\langle \rangle$ | < | | | | |
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| It is also the WEB signal of MPU interface.24, 48, 49, 66, 74, 76, 78N/ANCNot Connect These pins should be left open.9,60PowerVDDMSSDRAM Power Supply (3.3V)59,11PowerGNDMSSDRAM Ground10,42PowerDVDDDigital Power Supply (1.8V)45PowerDGNDDigital Ground23, 46, 73, 77PowerAVDDAnalog Power Supply (3.3V)22, 47, 75, 79PowerAGNDAnalog Ground | | | | | | | |
| 66, 74, 76, 78These pins should be left open.9,60PowerVDDMSSDRAM Power Supply (3.3V)59,11PowerGNDMSSDRAM Ground10,42PowerDVDDDigital Power Supply (1.8V)45PowerDGNDDigital Ground23, 46, 73, 77PowerAVDDAnalog Power Supply (3.3V)22, 47, 75, 79PowerAGNDAnalog Ground | | | $\langle \frown \rangle$ | | | | |
| 78Image: Non-transform9,60PowerVDDMSSDRAM Power Supply (3.3V)59,11PowerGNDMSSDRAM Ground10,42PowerDVDDDigital Power Supply (1.8V)45PowerDGNDDigital Ground23, 46, 73, 77PowerAVDDAnalog Power Supply (3.3V)22, 47, 75, 79PowerAGNDAnalog Ground | 24, 48, 49, | N/A | NC | Not Connect | | | |
| 9,60PowerVDDMSSDRAM Power Supply (3.3V)59,11PowerGNDMSSDRAM Ground10,42PowerDVDDDigital Power Supply (1.8V)45PowerDGNDDigital Ground23, 46, 73, 77PowerAVDDAnalog Power Supply (3.3V)22, 47, 75, 79PowerAGNDAnalog Ground | | | $ \searrow \checkmark /$ | These pins should be left open. | | | |
| 59,11PowerGNDMSSDRAM Ground10,42PowerDVDDDigital Power Supply (1.8V)45PowerDGNDDigital Ground23, 46, 73, 77PowerAVDDAnalog Power Supply (3.3V)22, 47, 75, 79PowerAGNDAnalog Ground | | | | | | | |
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| 45PowerDGNDDigital Ground23, 46, 73, 77PowerAVDDAnalog Power Supply (3.3V)22, 47, 75, 79PowerAGNDAnalog Ground | | | | | | | |
| 23, 46, 73, 77 Power AVDD Analog Power Supply (3.3V) 22, 47, 75, 79 Power AGND Analog Ground | | | | | | | |
| 77 22, 47, 75, Power AGND Analog Ground 79 AGND Analog Ground | | | | | | | |
| 79 | | Power | AVDD | Analog Power Supply (3.3V) | | | |
| | | Power | AGND | Analog Ground | | | |
| | | Power | VDDH | DVI Power Supply (3.3V) | | | |

| Pin # | Туре | Symbol | Description |
|-------|-------|----------|---|
| 33,38 | Power | VSSH | DVI Ground |
| 53,61 | Power | VDDMQ | SDRAM output buffer Power Supply (3.3V) |
| 52,62 | Power | GNDMQ | SDRAM output buffer Ground |
| 71 | Power | AVDD_PLL | PLL Power Supply (1.8V) |
| 70 | Power | AGND_PLL | PLL Ground |
| 83 | Power | VDDIO | IO Power Supply (1.2-3.3V) |

2.0 PACKAGE DIMENSIONS

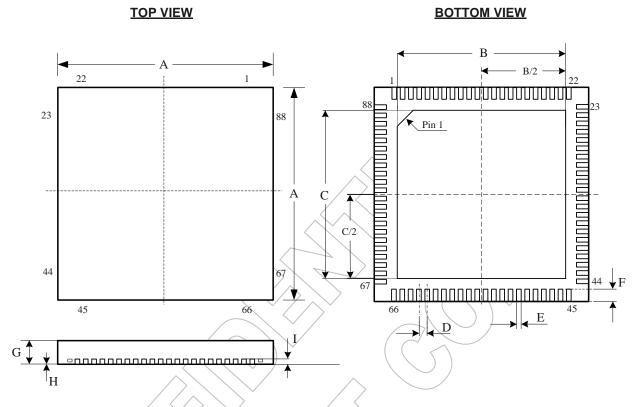


Figure 3: 88 Pin QFN Package (10 x 10 mm)

| No. of | Leads | $\overline{\frown}$ | / | \sim | \bigcirc | SYMBOL | 4 | | | |
|----------|--------|---------------------|------|--------|------------|--------|------|------|------|------|
| 88 (10 X | 10 mm) | A | В | ∕_C∕ | D | Е | F | G | Н | Ι |
| M:W | MIN | 9.90 | 6.65 | 6.65 | 0.30 | 0.15 | 0.40 | 0.80 | 0 | |
| Milli- | NOM | 10.00 | 6.75 | 6.75 | 0.40 | 0.20 | 0.50 | 0.85 | - | 0.20 |
| meters - | MAX | 10.10 | 6.85 | 6.85 | 0.50 | 0.25 | 0.60 | 0.90 | 0.05 | |

Table of Dimensions

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

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| ORDERING INFORMATION | | | | | | |
|----------------------|------------------|-----------------------------|------------------------|--|--|--|
| Part Number | Package Type | Operating Temperature Range | Minimum Order Quantity | | | |
| CH7035B-BF | 88QFN, Lead-free | Commercial : -20 to 70°C | 168/Tray | | | |
| CH7035B-BFI | 88QFN, Lead-free | Industrial :-40 to 85°C | 168/Tray | | | |

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